MOSFET HAVING A JFET EMBEDDED AS A BODY DIODE

CROSS-REFERENCE TO RELATED APPLICATIONS

This Application claims the benefit of U.S. Provisional Patent Application No. 60/579,020 filed Jun. 10, 2004.

BACKGROUND OF THE INVENTION

Referring to FIG. **1**, a cross sectional view of a trench metal-oxide-semiconductor field effect transistor (TMOSFET) **100** according to the conventional art is shown. The TMOSFET **100** includes a source contact **110**, a plurality of source regions **115**, a plurality of gate regions **120**, a plurality of gate insulator regions **125**, a plurality of body regions **130**, **135** a drain region **140**, **145** and drain contact **150**. The drain region **140**, **145** may optionally include a first drain region **140** and a second drain region **145**. The body regions may optionally include first body regions **130** and second body regions **135**.

The body regions **130**, **135** are disposed above the drain region **140**, **145**. The source regions **115**, gate regions **120** and the gate insulator regions **125** are disposed within the body regions **130**. The gate regions **120** and the gate insulator regions **125** may extend into a portion of the drain region **140**, **145**. The gate regions **120** and the gate insulator regions **125** are formed as parallel-elongated structures. The gate insulator regions **125** surround the gate regions **120**. Thus, the gate regions **120** are electrically isolated from the surrounding regions by the gate insulator regions **125**. The gate regions **120** are coupled to form a common gate of the device **100**. The source regions **115** are coupled to form a common source of the device **100**, by the source contacts **110**. The source contact **110** also couples the source regions **115** to the body regions **130**, **135**.

The source regions **115** and the drain regions **140**, **145** may be n-doped (N) semiconductor such as silicon doped with Phosphorus or Arsenic. The body regions **130**, **135** may be p-doped (P) semiconductor, such as silicon doped with Boron. The gate region **120** may be n-doped (N) semiconductor, such as polysilicon doped with Phosphorus. The gate insulator regions **125** may be an insulator, such as silicon dioxide.

When the potential of the gate regions **120**, with respect to the source regions **115**, is increased above the threshold voltage of the device **100**, a conducting channel is induced in the body regions **130**, **135** along the periphery of the gate insulator regions **125**. The TMSOFET **100** will then conduct current between the drain region **140**, **145** and the source regions **115**. Accordingly, the device is in its on state.

When the potential of the gate regions **120** is reduced below the threshold voltage, the channel is no longer induced. As a result, a voltage potential applied between the drain region **140**, **145** and the source regions **115** will not cause current to flow there between. Accordingly, the device **100** is in its off state and the junction formed by the body regions **130**, **135** and the drain region **140**, **145** supports the voltage applied across the source and drain.

If the drain region **135**, **140** includes a first drain region **140** disposed above a second drain region **145**, the first drain region **140** is lightly n-doped (N−) semiconductor, such as silicon doped with Phosphorus or Arsenic, and the second drain region **145** is heavily n-doped (N+) semiconductor, such as silicon doped with Phosphorus or Arsenic. If the body regions **130**, **135** include first body regions **130** disposed between the source regions **115** and the first drain region **140** proximate the gate regions **120**, the first body regions **130** are moderately to lightly p-doped (P or P−) semiconductor, such as silicon doped with Boron, and the second body regions **235** are heavily p-doped (P+) semiconductor, such as silicon doped with Boron. The first drain region **140** and the first body regions **130** reduce the punch through effect. Accordingly, the first drain region **140** and the first body regions **130** act to increase the breakdown voltage of the TMOSFET **100**.

Referring now to FIG. **2**, a cross sectional view of a non-trench based metal-oxide-semiconductor field effect transistor (MOSFET) **200** according to the conventional art is shown. The MOSFET **200** includes a source contact **210**, a plurality of source regions **215**, a plurality of gate regions **220**, a plurality of gate insulator regions **225**, a plurality of body regions **230**, **235** a drain region **240**, **245** and a drain contact region **250**. The drain region **240**, **245** may optionally include a first drain region **240** and a second drain region **245**. The body regions **230**, **235** may optionally include first body regions **230** and second body regions **235**.

The source regions **215** are formed as parallel elongated structures disposed above the drain region **240**, **245**. The body regions **230**, **235** are disposed between the source regions **215** and the drain region **240**, **245**. The gate regions **220** are disposed above the drain regions **240**, **245** and the body regions **230**, **235**. The gate regions **220** are disposed between the source regions **215** above the drain regions **240**, **245**. Accordingly, a portion of the drain region **240**, **245** is disposed between the body regions **230**, **235** proximate the gate regions **220**. The gate insulator regions **225** surround the gate region **220**. Thus, the gate regions **220** are electrically isolated from the surrounding regions by the gate insulator regions **225**. The gate regions **220** may be coupled to form a common gate of the device **200**. The source contact **210** may be disposed on the source regions **215** and the body regions **230**, **235**. The source regions **215** may be coupled to form a common source of the device **200**, by the source contact **210**. The source contact **210** also couples the source regions **215** to the body regions **230**, **235**.

The source regions **215** and the drain region **240**, **245** may be n-doped semiconductor, such as silicon doped with Phosphorus or Arsenic. The body regions **230**, **235** may be p-doped semiconductor, such as silicon doped with Boron. The gate regions **220** may be n-doped semiconductor, such as polysilicon doped with Phosphorus. The gate insulator region **225** may be an insulator, such as silicon dioxide.

When the potential of the gate regions **220**, with respect to the source regions **215**, is increased above the threshold voltage of the device **200**, a conducting channel is induced in the body regions **230**, **235** between the source regions **215** and the drain region **240**, **245** proximate the gate regions **220**. The MOSFET **200** will then conduct current between the drain region **240**, **245** and the source regions **215**. Accordingly, the device **200** is in its one state.

When the potential of the gate regions **220** is reduced below the threshold voltage, the channel is no longer induced. As a result, a voltage potential applied between the drain region **240**, **245** and the source regions **215** will not cause current to flow there between. Accordingly, the device **200** is in its off state and the junction formed by the body regions **230**, **235** and the drain region **240**, **245** supports the voltage applied across the source and drain.

If the drain region **240**, **245** includes a first drain region **240** disposed above a second drain region **245** proximate the body regions **230**, **235** and the gate regions **220**, the first drain region **240** is moderately to lightly n-doped (N or N−) semiconductor and the second drain region **245** is heavily n-doped